TS32MLS72V6D

168PIN PC133 Unbuffered DIMM
256MB With 16Mx8 CL3

Description

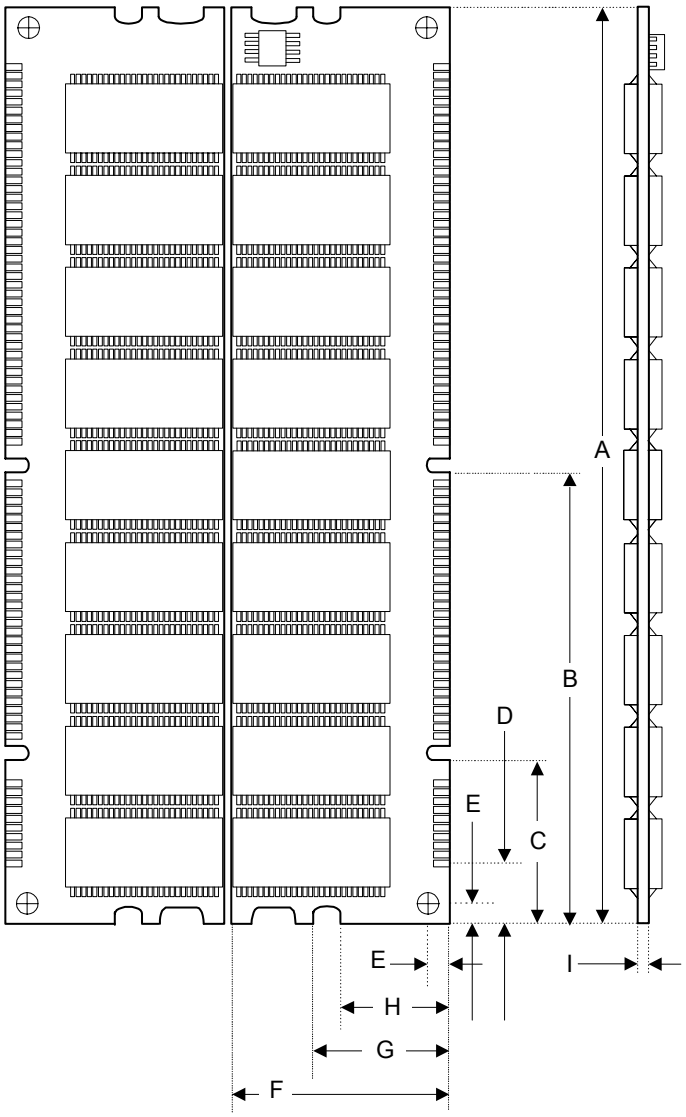
The TS32MLS72V6D is a 32M x 72bits Synchronous Dynamic RAM high-density for PC-133. The TS32MLS72V6D consists of 18pcs CMOS 16Mx8 bits Synchronous DRAMs in TSOP-II 400mil packages and a 2048 bits serial EEPROM on a 168-pin printed circuit board. The TS32MLS72V6D is a Dual In-Line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- Performance Range : PC-133 CL3
- Conformed to JEDEC Standard Spec.
- Burst Mode Operation.
- Auto and Self Refresh.
- CKE Power Down Mode.
- DQM Byte Masking (Read/Write)
- Serial Presence Detect (SPD) with serial EEPROM
- LVTTL compatible inputs and outputs.
- Single 3.3V ± 0.3V power supply.
- MRS cycle with address key programs.
  Latency (Access from column address)
  Burst Length (1,2,4,8 & Full Page)
  Data Sequence (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.

Placement



PCB :09-7149

Dimensions

Side	Millimeters	Inches
A	133.35±0.40	5.250±0.016
B	65.67	2.585
C	23.49	0.925
D	8.89	0.350
E	3.00	0.118
F	31.75±0.20	1.250±0.008
G	19.80	0.780
H	15.80	0.622
I	1.27±0.10	0.050±0.004

(Refer Placement)

Pin Identification

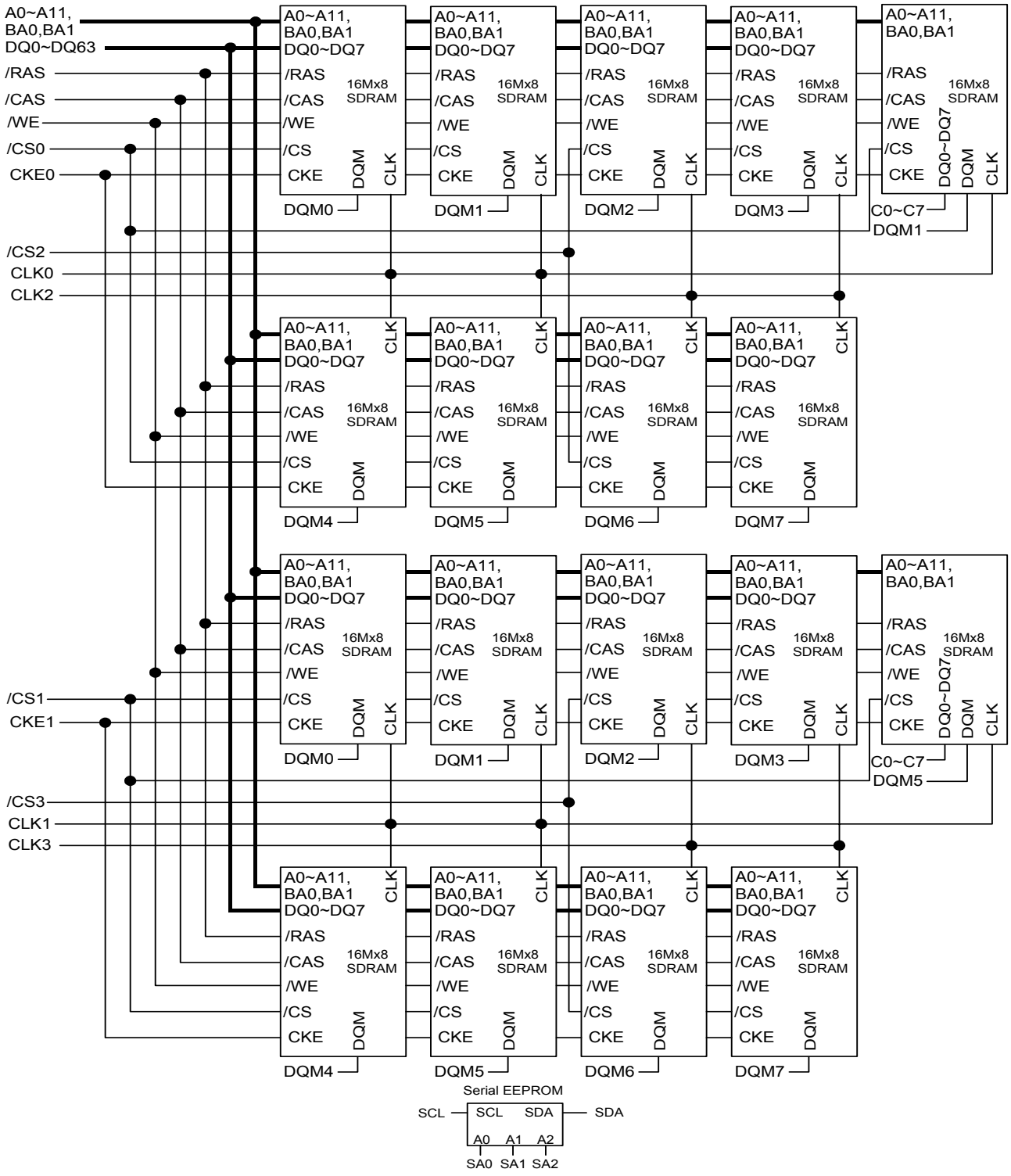
Symbol	Function
A0~A11, BA0, BA1	Address input
DQ0~DQ63, C0~C7	Data Input / Output.
CLK0~CLK3	Clock Input.
CKE0, CKE1	Clock Enable Input.
/CS0~/CS3	Chip Select Input.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DQM0~DQM7	Data (DQ) Mask
SA0~SA2	Address in EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
Vcc	+5.0 Voltage Power Supply
Vss	Ground
NC	No Connection

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	Vss	43	Vss	85	Vss	127	Vss
02	DQ0	44	NC	86	DQ32	128	CKE0
03	DQ1	45	/CS2	87	DQ33	129	*/CS3
04	DQ2	46	DQM2	88	DQ34	130	DQM6
05	DQ3	47	DQM3	89	DQ35	131	DQM7
06	Vcc	48	NC	90	Vcc	132	*A13
07	DQ4	49	Vcc	91	DQ36	133	Vcc
08	DQ5	50	NC	92	DQ37	134	NC
09	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	*C2	94	DQ39	136	*C6
11	DQ8	53	*C3	95	DQ40	137	*C7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	*Vref	104	DQ47	146	*Vref
21	*C0	63	*CKE1	105	*C4	147	*REGE
22	*C1	64	Vss	106	*C5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE	69	DQ24	111	/CAS	153	DQ56
28	DQM0	70	DQ25	112	DQM4	154	DQ57
29	DQM1	71	DQ26	113	DQM5	155	DQ58
30	/CS0	72	DQ27	114	*/CS1	156	DQ59
31	NC	73	Vcc	115	/RAS	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	*CLK2	121	A9	163	*CLK3
38	A10/AP	80	NC	122	BA0	164	NC
39	BA1	81	NC	123	A11	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	*CLK1	167	SA2
42	CLK0	84	Vcc	126	*A12	168	Vcc

*** Please refer Block Diagram**

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0~4.6	V
Voltage on V_{DD} supply to Vss	V_{DD}, V_{DDQ}	-1.0~4.6	V
Storage temperature	T_{STG}	-55~+150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA
Mean time between failure	MTBF	50	year
Temperature Humidity Burning	THB	85°C/85%, Static Stress	°C-%
Temperature Cycling Test	TC	0°C ~ 125°C Cycling	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max		Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	IOH=-2mA
Output low voltage	V_{OL}	-	-	0.4	V	IOL=2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

1. V_{IH} (max) = 5.6V AC .The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC .The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200mV)

	Symbol	Min	Max	
Address (A_0 ~A_{11}, BA_0 ~BA_1)	C_{ADD}	50	95	pF
/RAS, /CAS, /WE	C_{IN}	50	95	pF
CKE (CKE0 ~ CKE1)	C_{CKE}	28	50	pF
Clock (CLK0 ~ CLK3)	C_{CLK}	18	25	pF
/CS (/CS0 ~ /CS3)	C_{CS}	18	30	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	13	20	pF
DQ (DQ0 ~ DQ63)	C_{OUT1}	13	18	pF
CB (CB0 ~ CB7)	C_{OUT2}	13	18	pF

DC CHARACTERISTICS

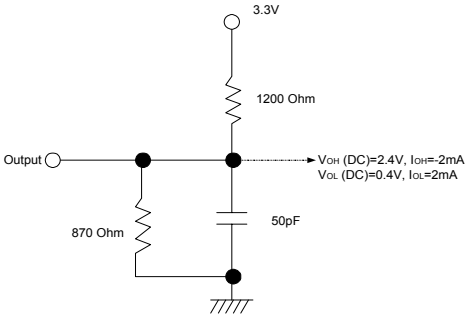
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Value	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_O=0mA	1,080	mA	1
Precharge Standby Current in power-down mode	I_{CC2}**P**	CKE≤V_{IL}(max), t_{CC}=10ns	36	mA	
	I_{CC2}**PS**	CKE & CLK≤V_{IL}(max), t_{CC}=∞	36		
Precharge Standby Current in non power-down mode	I_{CC2}**N**	CKE≥V_{IH}(min), /CS≥V_{IH}(min), t_{CC}=10ns Input signals are changed one time during 20ns	360	mA	
	I_{CC2}**NS**	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable	180		
Active Standby Current in power-down mode	I_{CC3}**P**	CKE≤V_{IL}(max), t_{CC}=10ns	90	mA	
	I_{CC3}**PS**	CKE & CLK≤V_{IL}(max), t_{CC}=∞	90		
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3}**N**	CKE≥V_{IH}(min), /CS≥V_{IH}(min), t_{CC}=10s Input signals are changed one time during 30ns	540	mA	
	I_{CC3}**NS**	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable	450		
Operating Current (Bust Mode)	I_{CC4}	I_{OL}= 0 mA Page Burst 4 Banks activated t_{CCD} = 2CLKs	1,620	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	2,070	mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V	36	mA	

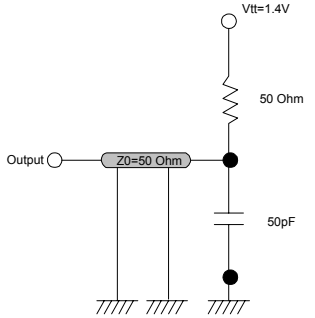
1. Measured with outputs open.
2. Refresh period is 64ms
3. Unless otherwise noted, input swing level is CMOS ($V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf=1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Value	Unit	Note
Row active to row active delay	t_{RRD}(min)	15	ns	1
/RAS to /CAS delay	t_{RCD}(min)	20	ns	1
Row precharge time	t_{RP}(min)	20	ns	1
Row active time	t_{RAS}(min)	45	ns	1
	t_{RAS}(max)	100	us	
Row cycle time	t_{RC}(min)	65	ns	1
Last data in to row precharge	t_{RDL}(min)	2	CLK	2
Last data in to Active precharge	t_{DAL}(min)	2 CLK + 20ns	-	
Last data in to new col. address delay	t_{CDL}(min)	1	CLK	2
Last data in to burst stop	t_{BDL}(min)	1	CLK	2
Col. address to col. address delay	t_{CCD}(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	-		

clock cycle time, and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	Min	Max	Unit	Note
CLK cycle time	CAS latency=3	t_{CC}	7.5	1000	ns	1
	CAS latency=2		-			
CLK to valid output delay	CAS latency=3	t_{SAC}	-	5.4	ns	1, 2
	CAS latency=2		-	-		
Output data hold time	CAS latency=3	t_{OH}	3	-	ns	2
	CAS latency=2		-	-		
CLK high pulse width		t_{CH}	2.5	-	ns	3
CLK low pulse width		t_{CL}	2.5	-	ns	3
Input setup time		t_{SS}	1.5	-	ns	3
Input hold time		t_{SH}	0.8	-	ns	3
CLK to output in Low-Z		t_{SLZ}	1	-	ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}	-	5.4	ns	
	CAS latency=2		-	-		

Note: 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_0~A_9	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down	Entry		H	L	H	X	X	X	X	X			
					L	V	V	V					
	Exit		L	H	X	X	X	X	X				
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X	X			
					L	H	H	H					
	Exit		L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

1. OP Code : Operand Code

3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatically precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at both banks precharge state.
4. BA_0~BA_1: Bank select address.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
   If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.

   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edged of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Serial Presence Detect Specification

Serial Presence Detect			
Byte No.	Function Described	Standard Specification	Vendor Part
0	Number of Bytes Written into Serial Memory	128bytes	80
1	Total # of Bytes of S.P.D Memory	256bytes	08
2	Fundamental Memory Type	SDRAM	04
3	Number of Row Addresses on this Assembly	12	0C
4	Number of Column Addresses on this Assembly	10	0A
5	Number of Module Rows on this Assembly	2 rows	02
6	Data Width of this Assembly	72bits	48
7	Data Width of this Assembly	-	00
8	Voltage Interface Standard of this Assembly	LVTTL	01
9	SDRAM Cycle Time @CAS latency of 3	7.5ns	75
10	SDRAM Access Time from Clock @CAS latency of 3	5.4ns	54
11	DIMM configuration type	ECC	02
12	Refresh Rate Type	15.625us/Self Refresh	80
13	Primary SDRAM Width	X8	08
14	Error Checking SDRAM Width	X8	08
15	Min Clock Delay for Back to Back Random Address	tCCD=1CLK	01
16	SDRAM Device Attributes: Burst Lengths Supported	1,2,4,8 & Full page	8F
17	SDRAM Device Attributes: # of banks on SDRAM device	4 bank	04
18	SDRAM Device Attributes: CAS Latency	2,3	06
19	SDRAM Device Attributes: CS Latency	0 clock	01
20	SDRAM Device Attributes: Write Latency	0 clock	01
21	SDRAM Module Attributes	Non-buffered, non-registered & redundant addressing	00
22	SDRAM Device Attributes: General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0E
23	SDRAM Cycle Time @CAS Latency of 2	10ns	A0
24	SDRAM Access Time from Clock @CAS Latency of 2	6ns	60
25	SDRAM Cycle Time @CAS Latency of 1	-	00
26	SDRAM Access Time from Clock @CAS Latency of 1	-	00
27	Minimum Row Precharge Time (=t RP)	20ns	14
28	Minimum Row Active to Row Activate (=t RRD)	15ns	0F
29	Minimum RAS to CAS Delay (=t RCD)	20ns	14
30	Minimum Activate Precharge Time (=t RAS)	45ns	2D
31	Module Row Density	2 rows of 128MB	20
32	Command and Address Signal input Setup Time	1.5ns	15
33	Command and Address Signal input Hold Time	0.8ns	08
34	Data Signal Setup Time	1.5ns	15
35	Data Signal Hold Time	0.8ns	08
36-61	Superset Information	-	00

62	SPD Data Revision Code	JEDEC2	02
63	Checksum for Bytes 0-62	-	B2
64-71	Manufacturers JEDEC ID Code per JEP-108E	Transcend	7F, 4F
72	Manufacturing Location	T	54
73-90	Manufacturers Part Number	TS32MLS72V6D	54 53 33 32 4D 4C 53 37 32 56 36 44 20 20 20 20 20 20
91-92	Revision Code	-	0
93-94	Manufacturing Date	By Manufacturer	Variable
95-98	Assembly Serial Number	By Manufacturer	Variable
99-125	Manufacturer Specific Data	-	0
126	Intel Specification Frequency	-	64
127	Intel Specification CAS# Latency/Clock Signal Support	CL=2, 3 Clock 0	F6
128~	Unused Storage Locations	Open	FF